IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Date: December 19, 2002

Misbahul Azam et al.

Serial No.: 09/705,274 Group Art Unit (2823)

Filed: November 3, 2000 Examiner: Khiem D. Nguyen

For: **TRENCH GROWTH TECHNIQUES USING SELECTIVE EPITAXY**

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS FACSIMILE TRANSMITTED TO THE PATENT AND TRADEMARK OFFICE AT THE FAX NO. (703) 872-9319 ADDRESSED TO:
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SEMICONDUCTOR COMPONENTS INDUSTRIES, L.L.C.
Name of Assignee

16 pages

Lydia McNamara 9/4/03
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REQUEST REINSTATEMENT OF APPEAL

Honorable Commissioner of Patents and Trademarks,
Washington D.C. 20231

SIR:

Applicant respectfully requests reinstatement of the appeal for the above application per 37 CFR 1.193 (b)(2)(ii).

A Supplemental Appeal Brief is filed concurrently with this request.

Respectfully submitted,
Misbahul Azam et al. by

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Date: Sept. 4, 2003

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SUPPLEMENTAL APPEAL BRIEF

Honorable Commissioner of Patents and Trademarks,
Washington D.C. 20231

SIR:

Please consider the following Supplemental Appeal Brief for the above identified patent application assigned to Semiconductor Components Industries, L.L.C.

I. REAL PARTY OF INTEREST

The subject application is assigned to SEMICONDUCTOR COMPONENTS INDUSTRIES, L.L.C., the real party of interest.

II. RELATED APPEALS AND INTERFERENCES

An Appeal Brief in the instant patent application was filed on December 19, 2002. There are no other related appeals or interferences.

III. STATUS OF THE CLAIMS

1. Claims 1-25 remain in the application and are the claims on appeal. A copy of these claims is provided in Appendix A.

2. Claims 1-27 were filed with the original application.

3. In an office action mailed on February 14, 2002, claims 1-26 were rejected under 35 U.S.C. § 102(a) as being anticipated by Madson (U.S. Publication No. US2001/0049167 A1). Claim 27 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Madson in combination with Williams et al. (U.S. Patent No. 6,239,463). In an amendment dated May 14, 2002, claims 1, 2, 9, 17 and 25 were amended, and claims 26-27 were cancelled. A final rejection mailed on October 15, 2002, rejected claims 1-25 under 35 U.S.C. § 103(a) as being unpatentable over Madson in view of Williams et al.

4. Applicants appealed, and on December 19, 2002, filed an appeal brief. The examiner responded by withdrawing the grounds for rejection and rejecting all claims on new grounds presented in the detailed action mailed June 6, 2003.

IV. STATUS OF AMENDMENTS FILED SUBSEQUENT TO FINAL REJECTION

A response to the final rejection was submitted on September 17, 2002, but no claims were amended. An advisory action confirming the rejection of claims 1-25 was mailed on October 15, 2002, indicating that the application was not in condition for allowance. Subsequent to the advisory action, a Notice of Appeal was faxed October 25, 2002, concurrently with a Petition for Extension of Time under 37 C.F.R. §1.136(a) to extend the period for response to November 17, 2002.

IV. SUMMARY OF THE INVENTION

The present invention relates to a method of forming a trench in semiconductor devices. Trench formation is known to affect device performance by reducing the device's voltage breakdown and increasing its drain-gate capacitance. In one embodiment, a masking material (14) is disposed on the semiconductor device, and a protruding portion (18) is formed at a trench location by forming an opening (20) in the masking material adjacent to the trench location. A semiconductor material (24) is deposited to fill in the opening and the protruding portion is removed to form the trench (26). The semiconductor material is etched to round off corners (28) of the trench.

As described in the Background of the Invention, page 1, line 7, through page 2, line 15, during the process used to manufacture trench semiconductor devices, a dry plasma silicon etch step typically is used to form the trenches in a silicon material. These processes must precisely control depth and not damage the channel region which is formed along the trench wall. Such damage can cause leakage and reduced carrier lifetime in the channel area, thereby increasing the voltage threshold and on-state resistance of the semiconductor device. The trench depth typically is a critical dimension which is difficult to control using dry silicon etch processes. For example, a trench power MOSFET device should have the trench depth just below the diffused body region to minimize the gate to drain capacitance and minimize the gate oxide electric field strength.

Applicants found that by using a dielectric masking material (18) such as an oxide or nitride to define a trench (26), depositing semiconductor material (24) in openings in the masking material, removing the masking material to form the trench (using a simple non-damaging mask removal process), a trench is produced that has a precisely controlled depth and little or no sidewall damage, which allows a high quality, repeatable channel to be formed along the trench sidewalls. Moreover, the claimed method does not disturb dopants (30) along the sidewall channel region, which results in better process control. The controlled trench depth and substantially damage free channel region improve the electrical performance of the semiconductor device. Additionally, a simple wet etch trench rounding process is performed to round the corners of the trench above the foundation layer (12) to reduce field stress and increase the device's breakdown voltage.

VI. ISSUE

Whether claims 1-25 are patentable under 35 U.S.C. § 103(a) over Madson (U.S. Publication No. 2001/0049167 A1) in view of Lowrey et al. (U.S. Patent No. 5,013,680).

VII. GROUPING OF THE CLAIMS

Appellants offer no other grouping of claims.

VIII. ARGUMENT

The Examiner rejected Claims 1-25 under 35 U.S.C. §103(a) over Madson in view of Lowrey et al. (Lowrey).

Claim 1 recites a method of forming a trench in a semiconductor device, comprising, among other things, forming a protruding portion (18) in a masking material (14), depositing a semiconductor material (24), removing the protruding portion to form the trench, and etching the semiconductor material to round off corners of the trench.

The Madson reference discloses several methods of manufacturing a high voltage trench transistor in which a semiconductor material (figure 8A, 802) is deposited in a region defined by a dielectric pillar (figure 8B, 806). The height of the dielectric pillar is reduced by plasma etching to leave a shorter dielectric pillar, i.e., a dielectric plug ("OX" of Fig. 8D) of a predetermined thickness (reference paragraphs 0007, 0010, 0011, 0013, 0014, 0028, 0035, 0039, 0041, 0044, 0056, 0058, 0060, 0062 and 0070). The Madson trench (i.e., figure 8D, 810) is formed over the shortened dielectric plug OX. The presence of dielectric

plug OX is the feature that provides the Madson trench device with a high breakdown voltage and a low drain to gate capacitance. The low capacitance promotes fast switching speeds.

The Lowrey reference discloses a method of forming a DRAM device in a trench 71. A protruding portion 31 is formed at a location of the trench by forming an opening in a masking material. Silicon dioxide is deposited to fill in the opening, and the protruding portion is removed to form a mask 51 using the remaining silicon dioxide. Exposed semiconductor material is etched through mask 51 to form trench 71 having rounded corners in an epi layer. The Lowrey et al. process of forming a mask 51, and etching semiconductor material through the mask to form trench 71 is employed to increase DRAM cell density (c2, lines 23-40). It is understood that DRAM devices operate at supply voltages of about five volts or less and therefore are considered low voltage devices. Moreover, a design goal of a DRAM is to provide a high capacitance per cell since the cell information is stored on the cell capacitance.

As indicated by the examiner in the June 6, 2003, office action, the Madson process reduces the height of, but does not remove, protruding dielectric pillar 806 to form a reduced height dielectric pillar or dielectric plug OX. All of the Madson devices are shown with the trench overlying dielectric plug OX. Nowhere in the Madson specification is any teaching provided or suggestion made to remove the dielectric pillar rather than reduce its height. Indeed, dielectric plug OX is the primary feature that provides the Madson et al. device with a high voltage breakdown and low capacitance. To remove it completely would defeat the purpose of the Madson device.

Madson in view of Lowrey fails to make claim 1 obvious because one skilled in the art would not be motivated to combine them. Obviousness cannot be established by combining the teaching of the prior art to produce the claimed invention absent, among other things, incentive supporting the combination. ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1576, 221 USPQ 929, 933 (Fed. Cir. 1984). When a 35 U.S.C. § 103 rejection is based upon a modification of a reference that destroys the intent or purpose of the invention disclosed in the reference, such a proposed modification is not proper and a prima facie case of obviousness cannot be properly made.

There is no motivation disclosed in the Madson reference for etching a trench to round off corners of the trench. In order to round the corners of the Madson trench, the shortened dielectric plug OX would have to be removed to prevent any etchant from undercutting to form detrimental voids along the sides of dielectric plug OX. Dielectric plug OX is the very feature that allows the Madson device to achieve its desired high breakdown voltage and low drain to gate capacitance. Removing it completely would require additional processing steps and higher manufacturing costs in order to incorporate the Lowrey et al. process, and such added processing would merely restore the Madson device to the performance level it had lost when OX was removed.

Finally, even if the Madson device were combined with the Lowrey device and voids were not produced along the sides of the dielectric plug, the result would be a device having a protruding plug of oxide left from the pillar in the bottom of the trench, and would not have the advantage taught by the applicant of improved depth control, high voltage breakdown improvements and accurate alignment of the

trench bottom to the foundation layer (12) as described in the specification on page 7, line 15 through page 9, line 24. Furthermore, such a device would not have the rounded off semiconductor material on top of a foundation layer 12 as does the applicant. Instead, the rounding would occur on top of the Madson plug resulting in poor channel resistance.

The Examiner further states it would have been obvious to combine the teachings of Lowrey and Madson to "enable the trench having round off corners of Madson to augment uniform deposition of subsequent filling materials." However, the Examiner has not shown any basis in either Madson or Lowrey for combining or modifying either reference to support such a statement. Since the intended function of the Madson device would be destroyed if the shortened dielectric pillar were removed, Applicants submit that there is no such motivation. It is difficult to see where such motivation could lie since the Madson device is a high voltage transistor having low capacitance (to increase switching speeds), and the Lowrey DRAM is designed to operate at a low voltage while attempting to achieve a high capacitance in a small die area. Thus, the applicants believe there is no basis in these disparate arts to motivate combination of these references.

For at least the above reasons, applicants respectfully submit that Madson et al. in view of Lowrey et al. does not make claim 1 obvious, so that claim 1 should be allowable. Claims 2-8 depend directly or indirectly from claim 1 and are believed allowable for similar reasons.

Claims 9 and 17

Claim 9 calls for, among other things, removing a protruding region to form a trench within an epi layer and etching the epi layer to round off corners of the trench. Claim 17 calls for, among other things, removing a protruding region to form a trench and etching a material to round off corners of the trench.

For at least the reasons discussed above, there is no motivation disclosed in the references for Madson et al. to remove a protruding region to form a trench and to etch a material to round off corners of the trench.

Therefore, independent claims 9 and 17 are both believed allowable over Madson et al. in view of Lowrey et al. Claims 10-16 depend from claim 9 and claims 18-25 depend from claim 17, and so are believed allowable as well.

In view of the above, it is believed that claims 1-25 are allowable, and the case is now in condition for allowance, which action is earnestly solicited.

Respectfully submitted,
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Date: September 4, 2003

APPENDIX A

Claims

1. A method of forming a trench in a semiconductor device, comprising:

disposing a masking material on the semiconductor device;

forming a protruding portion at a location of the trench by forming an opening in the masking material adjacent to the location of the trench;

depositing a semiconductor material to fill in the opening;

removing the protruding portion to form the trench; and

etching the semiconductor material to round off corners of the trench.

2. The method of claim 1, further including:

providing a substrate supporting the masking material; and

forming a first epi layer between the substrate and the masking material.

3. The method of claim 1, wherein the semiconductor material is an epitaxial material.

4. The method of claim 1, further including the step of forming a mask at the location of the trench after disposing the masking material.

5. The method of claim 4, wherein forming the protruding portion further includes performing an etch step to remove the masking material where the mask is absent to form the opening.

6. The method of claim 1, wherein depositing the semiconductor material includes using a selective epi growth process to fill in the opening.

7. The method of claim 1, wherein depositing the semiconductor material includes using a blanket epi growth process to deposit the semiconductor material over the protruding portion and in the opening.

8. The method of claim 1, wherein removing the protruding portion step is a non-damaging mask removal step.

9. A method of forming a trench in a semiconductor device, comprising:

providing a substrate for the semiconductor device;

forming a first epi layer above the substrate and having a major surface;

forming a protruding region on the first epi layer having an opening adjacent to the protruding region and exposing the major surface of the first epi layer;

forming a second epi layer within the opening adjacent to the protruding region;

removing the protruding region to form the trench within the second epi layer aligned with the major surface of the first epi layer of the semiconductor device; and

etching the second epi layer to round off corners of the trench.

10. The method of claim 9, further including before forming the protruding region, forming a masking material above the first epi layer.

11. The method of claim 10, further including forming a mask on the masking material at a location for the trench;

12. The method of claim 11, wherein the mask is a photoresist material.

13. The method of claim 11, wherein forming the protruding region further includes performing an etch step to remove the masking material where the mask is absent to form the opening.

14. The method of claim 9, wherein forming the second epi layer includes using a selective epi growth process.

15. The method of claim 9, wherein forming the second epi layer further includes forming the second epi layer over the protruding region.

16. The method of claim 15, wherein forming the second epi layer over the protruding region includes using a blanket epi growth process.

17. A method of forming a trench in a semiconductor device, comprising;

disposing a first material on the semiconductor device;

forming first and second openings in the first material to form a protruding region;

disposing a second material in the first and second openings;

removing the protruding region to form the trench; and

etching the second material to round off corners of the trench.

18. The method of claim 17, further including:

forming a substrate below the first material; and

forming an epi layer between the substrate and the first material.

19. The method of claim 17, wherein the first material is a masking material from a group consisting of silicon dioxide and silicon nitride.

20. The method of claim 17, wherein the second material is an epitaxial material comprised of silicon.

21. The method of claim 17, further including forming a mask on the first material after disposing the first material.

22. The method of claim 21, wherein forming the first and second openings includes performing an etch step to remove the first material adjacent to the mask.

23. The method of claim 17, wherein disposing the second material includes using a selective epi growth process.

24. The method of claim 17, wherein disposing the second material further includes disposing the second material over the protruding region.

25. The method of claim 24, wherein disposing the second material over the protruding region includes using a blanket epi growth process.